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IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of the claims in the application:

1. (currently amended) A method of measuring signal skew ~~of a signal tree~~ on a programmable logic device, the device including a signal tree having a source node connected to first, second, and third destination branches, first, second, and third logic blocks programmably connectable to the respective first, second, and third destination branches, each of the logic blocks having an input terminal and an output terminal, the method comprising:

A3 Cont'd

a. instantiating a first delay element on the device using a first programming sequence that includes:
   i. connecting the first destination branch to the input terminal of the first logic block; and
   ii. connecting the output terminal of the first logic block to the input terminal of the second logic block; and

b. instantiating a second delay element on the device using a second programming sequence that includes:
   i. connecting the third destination branch to the input terminal of the third logic block; and
   ii. connecting the output terminal of the third logic block to the input terminal of the second logic block.

2. (original) The method of claim 1, wherein the signal tree is a clock tree.

3. (original) The method of claim 1, wherein the input terminal of the second logic block is an asynchronous input terminal.

4. (original) The method of claim 1, wherein the first, second, and third logic blocks are arranged on the device in a column.

5. (currently amended) The method of claim 4, wherein the second logic block is physically between the first and ~~second~~ third logic blocks.

A3 Cont'd

6. (original) The method of claim 1, wherein the source node is further connected to fourth, fifth, and sixth destination branches and the programmable logic device further includes fourth, fifth, and sixth logic blocks programmably connectable to the respective fourth, fifth, and sixth destination branches, each of the logic blocks having an input terminal and an output terminal, the method further comprising:

c. instantiating a third delay element on the device using a third programming sequence that includes:

i. connecting the fourth destination branch to the input terminal of the fourth logic block; and

ii. connecting the output terminal of the fourth logic block to the input terminal of the fifth logic block; and

b. instantiating a fourth delay element on the device using a fourth programming sequence that includes:

i. connecting the sixth destination branch to the input terminal of the sixth logic block; and

ii. connecting the output terminal of the sixth logic block to the input terminal of the fifth logic block.

7. (original) The method of claim 6, wherein connecting the output terminal of the first logic block to the input terminal of the second logic block establishes a first net, connecting the output terminal of the second logic

block to the input terminal of the second logic block establishes a second net, connecting the output terminal of the fourth logic block to the input terminal of the fifth logic block establishes a third net, and connecting the output terminal of the sixth logic block to the input terminal of the fifth logic block establishes a fourth net, the method further comprising defining the first and third nets to be identical and defining the second and fourth nets to be identical.

A3 Cont'd

8. (original) The method of claim 1, further comprising configuring the device to include the first and second delay elements in respective first and second oscillators.

9. (original) The method of claim 8, further comprising comparing the periods of the first and second oscillators.

Claims 10-18 (canceled).

19. (new) A method of measuring clock skew on a programmable logic device, the programmable logic device including a clock-distribution network having a source node connected to first, second, and third destination branches, and first, second, and third programmable logic blocks programmably connectable to the respective first, second, and third destination branches, each of the programmable logic blocks having an input terminal and an output terminal, the method comprising:

a. programming the programmable logic device to include a first ring oscillator in which the first destination branch is connected to the input terminal of the first logic block and the output terminal of the first logic block is connected to

the input terminal of the second logic block; and

b. programming the programmable logic device to include a second ring oscillator in which the third destination branch is connected to the input terminal of the third logic block and the output terminal of the third logic block is connected to the input terminal of the second logic block.

A3 Cont'd

20. (new) The method of claim 19, wherein the input terminal of the second logic block is an asynchronous input terminal.

21. (new) The method of claim 19, wherein the first, second, and third logic blocks are arranged on the programmable logic device in a column.

22. (new) The method of claim 21, wherein the second logic block is physically between the first and third logic blocks.

23. (new) The method of claim 19, wherein the source node is further connected to fourth, fifth, and sixth destination branches and the programmable logic device further includes fourth, fifth, and sixth programmable logic blocks programmably connectable to the respective fourth, fifth, and sixth destination branches, each of the programmable logic blocks having an input terminal and an output terminal, the method further comprising:

c. programming the programmable logic device to include a third ring oscillator in which the fourth destination branch is connected to the input terminal of the fourth logic block and the output terminal of the fourth logic block is connected to the input terminal of the fifth logic block; and

d. programming the programmable logic device to include

a fourth ring oscillator in which the sixth destination branch is connected to the input terminal of the sixth logic block and the output terminal of the sixth logic block to the input terminal of the fifth logic block.

A3 end

24. (new) The method of claim 23, wherein connecting the output terminal of the first logic block to the input terminal of the second logic block establishes a first net, connecting the output terminal of the second logic block to the input terminal of the second logic block establishes a second net, connecting the output terminal of the fourth logic block to the input terminal of the fifth logic block establishes a third net, and connecting the output terminal of the sixth logic block to the input terminal of the fifth logic block establishes a fourth net, the method further comprising defining the first and third nets to be identical and defining the second and fourth nets to be identical.

25. (new) The method of claim 19, further comprising configuring the programmable logic device to include the first and second delay elements in respective first and second oscillators.

26. (new) The method of claim 25, further comprising comparing the periods of the first and second oscillators.